IN THE SPECIFICATION

On page 1, line 2, please insert: --WITH OVERLAPPING GATES-- after "NON-VOLATILE SEMICONDUCTOR STORAGE APPARATUS".

Please rewrite the paragraphs beginning on page 19, line 17, and ending on page 20, line 27, as follows:

Then, a silicon oxide film is fully stacked, and the stacked film is etched back, whereby a side wall (not shown) is formed laterally of the gate electrode in the peripheral circuit region. At the same time, as shown in Fig. 7I, a side wall 18 composing of an oxide film is formed laterally of the polysilicon film 16, ONO film 15, and polysilicon film 13. Further, in the peripheral circuit region, the side wall is defined as a mask, and ion-implantation with high density is carried out, thereby forming a transistor with an LDD structure. Further, an interlayer insulation film 19 consisting of a BPSG (boron-doped phosphor-silicate glass) film, for example, is stacked by a CVD method. The thickness of the interlayer insulation film 19 is about 8000 to 10000 Angstroms, for example. Next, as shown in Fig. 8E, contact holes 20 reaching the N^+ diffusions 9b are formed in the interlayer insulation film 19 and silicon oxide film 11, wiring layers 21 are embedded in the contact holes 20, and a wiring layer 22 commonly connecting the wiring layers is further formed as a bit line BL. The wiring layers 21 and 22 are made of an aluminum alloy, for example, and the thickness of the wiring layer 22 is about 4000 to 6000 Angstroms, for example. As a source, a source line is formed commonly by the N^+ diffusion layer 9a. In addition, the N^+ diffusion layer 9b and wiring layer 21 are shared between the adjacent memory cell transistors in the columnar direction (transverse direction in Fig. 7I).